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L3: Entry 4 of 28 File: USPT Oct 30, 2001

DOCUMENT-IDENTIFIER: US 6311230 B1
TITLE: System and method for cell switching with a peripheral component interconnect bus and decentralized, computer-controlled cell switch

Detailed Description Text (26):
Turning now to FIG. 4, illustrated is an ATM cell format 400 having a 3 octet trailer according to the present invention. Those skilled in the art will recognize the basic cell format 400 as being based on the ATM Network Node Interface ("NNI") header format. Bytes (octets) 1 through 53 (comprising a virtual port identification ("VPI") field 410, a VCI field 420, a payload type ("PT") field 430, a cell loss priority ("CLP") field 440, a header error correction ("HEC") field 450 and a 48 octet payload field 460) constitute a standard ATM cell. Those skilled in the art understand that, in ATM parlance, VPIs and VCIs together identify a virtual circuit.

Detailed Description Text (36):
In a block 630, data to be switched in the cell switch arrive via an incoming line. In a block 640, the port card segments the data into 48 octet payloads and temporarily stores cells to be switched in its local memory. In a block 650, the 5 octet header is pre-appended and the 3 octet trailer is appended to the 48 octet payload. In a block 660, PCI bus master circuitry requests bus master status. In a block 670, bus master status is granted. The port card therefore has gained control of the bus to allow the interface circuitry of the port card to place the cells on the bus. In a block 680, the port card places the cells on the bus, preferably by placing the bus in a conventional burst mode. The cells are directly communicated from the interface circuitry to another port card in the cell switch via the bus, thereby relieving the host computer of having to switch the cells centrally. The cells are received into the inbound cell queue of the other port card and the PCI indices checked to establish the order and completeness of the cells.

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L3: Entry 4 of 28 File: USPT Oct 30, 2001

US-PAT-NO: 6311230
DOCUMENT-IDENTIFIER: US 6311230 B1

TITLE: System and method for cell switching with a peripheral component interconnect bus and decentralized, computer-controlled cell switch

DATE-ISSUED: October 30, 2001

INVENTOR-INFORMATION:

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ASSIGNEE-INFORMATION:

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APPL-NO: 08/ 998533 [PALM]
DATE FILED: December 26, 1997

PARENT-CASE:
CROSS-REFERENCE TO RELATED APPLICATION This Application claims the benefit of U.S. Provisional Application Ser. No. 60/034,451, filed on Dec. 27, 1996, and entitled "System and Method for Cell Switching with a Peripheral Component Interconnect Bus and Decentralized, Computer-Controlled Cell Switch," commonly assigned with the present invention and incorporated herein by reference.

INT-CL: [07] G06 F 3/00, G06 F 13/368, H04 L 12/28, H04 L 12/56

US-CL-ISSUED: 710/5; 710/119, 710/242, 370/396
US-CL-CURRENT: 710/5; 370/396, 710/119, 710/242

FIELD-OF-SEARCH: 709/201, 709/212, 709/231, 709/243, 710/119, 710/131, 710/242, 710/5, 370/390, 370/396

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4535453	August 1985	Rhodes et al.	370/110.1
☐	5450411	September 1995	Heil	370/94.2
☐	5689644	November 1997	Chou et al.	395/200.06
☐	5758109	May 1998	Gafford et al.	395/308
☐	5787095	July 1998	Myers et al.	371/68.1
☐	6072798	June 2000	Beasley	370/395
☐	6101184	August 2000	Tobe et al.	370/390

ART-UNIT: 212

PRIMARY-EXAMINER: Lee; Thomas

ASSISTANT-EXAMINER: Cao; Chun

ABSTRACT:

A port card employable in a cell switch including a host computer having a processor and a bus for interconnecting a plurality of port cards and a method of switching cells in the cell switch. The port card includes: (1) bus master circuitry for gaining control of the bus to allow the port card to place cells to be switched in the cell switch on the bus and (2) interface circuitry, coupled to the local memory and the bus master circuitry, that places the cells on the bus when the bus master circuitry has gained control of the bus, the cells communicated directly from the interface circuitry to another port card in the cell switch via the bus. The processor (or, more generally, the host computer) is relieved of having to participate directly in switching the cells.

21 Claims, 6 Drawing figures

L3: Entry 10 of 28 File: USPT Apr 6, 1999

DOCUMENT-IDENTIFIER: US 5892535 A
TITLE: Flexible, configurable, hierarchical system for distributing programming

Brief Summary Text (7):
As shown in FIG. 1, equipment, such as a network feed downlink 102 and a group of integrated receiver/decoders (or "IRDs") 104, at a cable headend location receives the transmitted signals that appear on a variety of different channels, and appropriately amplifies and conditions each of these signals (not shown). Then, equipment, such as a plurality of remodulators 106 and a channel combiner 108, remodulate and frequency division multiplex each of the resulting signals into a single broadband, frequency division multiplexed signal. This broadband signal is further amplified and driven (e.g., by distribution fan-out nodes 110) onto a geographically dispersed hardwired coaxial cable network for distribution to individual subscribers 112. Each subscriber 112 utilizes a converter (also commonly referred to as a "set-top box") which terminates a so-called cable "drop" in the network. Hence, the cable television headend station is often referred to as a "community antenna."

Detailed Description Text (91):
As discussed above with reference to FIG. 3, a distribution network interface unit 206 receives a channel of a network feed from an associated integrated receiver/decoder 210 for example. Each channel of the network feed will include cue tones. As shown in FIG. 11d, a cue tone decode process 1177, carried out by the cue tone DTMF decoder 726, bus 732, and microprocessor 728 for example, decodes received cue tone(s), formats it with a distribution network interface unit 206 identifier (and optionally, a server interface unit 204 identifier), and provides it to a control bus interface process 1183. The cue tone decode process 1177 may also determine whether the cue tone (e.g., consisting of DTMF.sub.-- VALUE.sub.-- 1, DTMF.sub.-- VALUE.sub.-- 2, DTMF.sub.--VALUE.sub.-- 3, DTMF.sub.--VALUE.sub.-- 4) is valid. That is, each distribution network interface unit 206 may be associated with a channel having a unique valid cue tone (e.g., CNN's valid cue tone may be: 1#5*). More specifically, referring to FIG. 7a, a cue tone dual tone multi-frequency (or "DTMF") decoder 726 decodes the cue tone and provides the decoded cue tone information to the microprocessor 728 via bus 732. The control bus interface process 1183, which may be carried out by the microprocessor 728, formats the cue tone information and puts it on the data bus 950 of the control bus 226. FIG. 29 illustrates an exemplary format for the decoded cue tone information packet 2900. As shown, the decoded cue tone information packet 2900 includes a cue tone header field 2902, a cue tone type field 2904, a server interface unit identifier field 2906, and a distribution network interface unit identifier field 2908. The cue tone header field 2902 includes a bit sequence which identifies the packet 2900. The cue tone type field 2904 identifies the cue tone as (a) a pre-roll cue tone, (b) a transfer-to-ad cue tone, or (c) a return cue tone. The cue tone (16.sup.4) value may also be provided. The server interface unit ID field 2906 and the distribution network interface unit ID field 2908 permit the channel receiving the cue tone to be uniquely identified.

Detailed Description Text (197):
The DS3/ATM daughter card 3128 includes an ATM segmentation and reassembly (or SAR) chip 3162, a DS3 physical interface chip 3166, a transmit FIFO 3168, a receive FIFO 3170, and a transmit data FIFO 3164. The streamer ATM input/output card 3130 includes a DS3 line interface unit 3172. The ATM SAR chip 3162 segments the MPEG-2

transport stream packets into ATM packets (of 53 bytes having a 48 byte payload). The microprocessor inserts required data, such as virtual path and virtual channel routing information, into the five byte header of each ATM packet. The ATM packets output by the ATM SAR 3162 are provided to the DS3 physical interface chip 3166 via transmit data FIFO 3164 which smoothes the bursts of data to the DS3 rate of 44.736 Mbps. The DS3 line interface unit 3172 is an electrical signal interface. The transfer and receive FIFOs 3168 and 3170, respectively, provide a control path from and to the microprocessor 3106 for sending and receiving control (non-transport stream) data.

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L3: Entry 10 of 28 File: USPT Apr 6, 1999

US-PAT-NO: 5892535
DOCUMENT-IDENTIFIER: US 5892535 A

TITLE: Flexible, configurable, hierarchical system for distributing programming

DATE-ISSUED: April 6, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Allen; Philip M.	Duluth	GA		
Davis; Joseph W.	Duluth	GA		
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Mai; Khanh	Alpharetta	GA		
Paulk; Howard L.	Cumming	GA		
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ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Digital Video Systems, Inc.	Los Gatos	CA			02

APPL-NO: 08/ 766569 [PALM]
DATE FILED: December 13, 1996

PARENT-CASE:
RELATED APPLICATIONS This invention is a continuation-in-part of U.S. patent application Ser. No. 08/646,657, entitled "MULTIPLE-SOURCE TRANSMISSION SYSTEM," filed on May 8, 1996, and commonly assigned.

INT-CL: [06] H04 N 7/10

US-CL-ISSUED: 348/9; 348/6, 455/4.2, 345/327
US-CL-CURRENT: 725/36; 345/716, 725/91, 725/93

FIELD-OF-SEARCH: 348/6, 348/7, 348/8, 348/9, 348/705, 348/706

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4814883	March 1989	Perine et al.	348/9 X
☐	5200825	April 1993	Perine	348/9 X
☐	5424770	June 1995	Schmelzer et al.	348/9
☐	5600366	February 1997	Schulman	348/9

ART-UNIT: 271

PRIMARY-EXAMINER: Flynn; Nathan

ATTY-AGENT-FIRM: Sawyer & Associates

ABSTRACT:

A flexible and configurable system for distributing media (or programming) to one or more distribution networks. The system includes a media server, at least one server interface unit, a first communications path coupling the media server and a server interface unit, distribution network interface unit(s), and a second communications path coupling a server interface unit and the distribution network interface unit(s). The media server stores files of encoded (e.g., compressed) media data and files of scheduling information. Each of the distribution network interface unit(s) conditions received media data for transmission over the distribution network(s) which may be analog and/or digital distribution networks.

66 Claims, 48 Drawing figures

L3: Entry 12 of 28 File: USPT Nov 24, 1998

DOCUMENT-IDENTIFIER: US 5841771 A
TITLE: Telecommunications switch apparatus and method for time switching

Drawing Description Text (30):
FIG. 27 is a block diagram wherein three of the basic switching systems illustrated in FIG. 25, coupled in accordance with the invention via an ATM cell switching node with one another and with a common call controller, a publicly accessible telecommunications network and multi-media messaging facilities;

Detailed Description Text (111):
The structure illustrated in FIG. 19 includes an ingress header processor 901 connected to receive incoming cell headers from the receive header bus 544. The ingress header processor 901 distinguishes headers of asynchronous payload cells and synchronous payload cells for routing to either of an asynchronous ingress processor 903 or a DS0 ingress processor 904 and a DS0/VP translation memory 905, via a header bus 930. The asynchronous ingress processor 903 is responsible for generating address information for writing the SRAMs 741 and 742 with asynchronous payloads to affect the FIFO memory function. An ingress/egress processor bidirectional bus 927 provides a communications link between the asynchronous ingress processor 903 and an egress scheduling processor 921. The egress scheduling processor 921 is linked via a DS0 transfer bus 931 to receive information from a DS0 buffer and transfer processor 906. The egress scheduling processor 921 stores and refers to egress scheduling information in an egress scheduling memory 922 via an egress scheduling memory bus 947. An asynchronous header memory 911 is connected to exchange data with the asynchronous ingress processor 903 and the egress scheduling processor 921 via an asynchronous header memory bus 928. The DS0 ingress processor 904 and the DS0 buffer and transfer processor 906 are both linked to communicate with the DS0/VP translation memory 905 by a DS0/virtual path translation memory (VPTM) bus 929; linked to communicate with an asynchronous pointer table 912 and a buffer pointer table 913 by a pointers bus 926; and linked to a buffer status memory 914 by a buffer status bus 925. Both the asynchronous pointer table 912 and the asynchronous header memory 911 are connected to receive address information from the asynchronous ingress processor 903 via the ingress/egress processor bidirectional bus 927. The DS0 buffer and transfer processor 906 provides DS0 connection memory write addressing information to a connection memory write generator 907. The connection memory write generator 907 generates the DS0 write channel connection memory pointers WCCMs, of 15 bits, onto the write address portion in the address bus B 542, for operation of the SRAMs 771 and 772 in FIG. 16. The DS0 buffer and transfer processor 906 also provides elastic store read address information on a buffer DS0 read address bus 938. The DS0 ingress processor 904 provides buffer write addressing information on a synchronous write address bus 937. The egress scheduling processor 921 provides egress headers (EHDR) on the transmit header bus 545, as well as providing address information on an asynchronous read address bus 936. A connection memory read generator 923 is responsive to the egress scheduling processor 921 for providing the read channel connection memory addresses RCCMs, of 15 bits, onto the read address portion in the address bus B 542, for storage in the SRAMs 741 and 742 in FIG. 16. A cell address generator 924 is connected to receive addressing information from each of the buses 935, 936, 937, and 938, and provide therefrom cell payload write memory pointers and cell payload read memory pointers, (CRWADDR) on the address bus A 543. Bidirectional information exchange with the micro controller unit 550 and the port circuit 518 at port 8 is provided by a micro controller bus access circuit 917. Timing signals for the operation of the memory

controller 580 are generated by a timing circuit 918 in response to the 25.7 ns clock signals CKL26 and the SONET frame pulse signal FP. Connection of the elements of FIG. 19 with the control bus access circuit 917 and the timing circuit 918 are provided via a microcontroller access bus 917a and a timing bus 918a; however as these connections will be apparent to persons of typical skill in the electronic switching or the electronic computer fields of technology, these connections are only further disclosed in those instances where such may be beneficial to an understanding of the control of the switching system.

Detailed Description Text (114):
The asynchronous ingress processor 903, in FIG. 19, is responsible for disposing of asynchronous cells that are designated as being one of, incoming reserved, outgoing reserved and valid asynchronous. The asynchronous ingress processor 903, as exemplified in FIG. 21, includes an asynchronous ingress controller 955 which is coupled to receive signals from; the incoming OA&M reserved cell flag lead 949, the outgoing OA&M reserved cell flag lead 950, the bad header interrupt lead 951, the clock lead CLK26 and a frame pulse lead 954. The asynchronous ingress controller 955 is also connected to communicate with the ingress/egress processor bidirectional bus 927, to communicate via a local control bus 955c, to communicate with the microprocessor access bus 917a, and to receive from the header bus 930. An asynchronous write pointer manager 956 is connected to receive from the header bus 930 and is connected to communicate with the microprocessor access bus 917a and the local control bus 955c. A header modify circuit 957 is connected to communicate with the microprocessor access bus 917a, and to receive from the header bus 930 and the local control bus 955c. The asynchronous write pointer manager 956 is connected to communicate with the asynchronous pointer table 912, shown in FIG. 19, via the pointers bus 926 and to send overflow signals to the asynchronous ingress controller 955 via an overflow lead 960. The asynchronous write pointer manager 956 is the source of asynchronous payload write addresses for the asynchronous write address bus 935 and the source of overflow interrupt signals on an overflow interrupt lead 962. Both the asynchronous write pointer manager 956 and the header modifier circuit 957 are connected to address the asynchronous pointer table 912 and the asynchronous header memory 911, shown in FIG. 19, via the read/write pointer access bus 927. The asynchronous write pointer manager 956 exchanges data with the asynchronous pointer table 912 via the pointers bus 926. The header modifier circuit 957 exchanges data with the asynchronous header memory 911 via the asynchronous header memory bus 928.

Detailed Description Text (115):
The DS0 ingress processor 904, in FIG. 19, generates write addressing information to be used in the capture of incoming synchronous payload data, and is shown in more detail in FIG. 22. A DS0 ingress controller 971 is coupled to receive signals; via the incoming OA&M reserved cell flag lead 949, the outgoing OA&M reserved cell flag lead 950, the bad header flag lead 951, the clock lead CLK26, the frame pulse lead 954, and an overflow lead 997. The DS0 ingress controller 971 is connected to receive signals from the header bus 930, to communicate with the microprocessor access bus 917a, and to provide timing and control signals via a local control bus 971c. A buffer status manager circuit 976 is connected to receive signals from the pointers bus 926 and the DS0/VPTM bus 929, and to communicate with the buffer status bus 925. A buffer write pointer manager circuit 972 is connected to receive signals from the header bus 930, to receive control signals from the local control bus 971c and to receive signals from the DS0/VPTM bus 929. The buffer write pointer manager circuit 972 is connected to communicate with the buffer status bus 925 and is also a driver of each of an overflow interrupt lead 979, the overflow lead 977 as well as the read/write pointer access bus 926. The buffer write pointer manager circuit 972 is the source of the synchronous payload write addressing information for the synchronous write address bus 937.

Detailed Description Text (116):
The DS0 buffer and transfer processor 906, in FIG. 19, generates read addressing information for extracting cell payloads from the asynchronous buffer memory 560, and is shown in more detail in FIG. 23. A buffer and transfer controller 981 is connected to drive the DS0/VPTM bus 929, to communicate control and timing signals via a local control bus 981c. The buffer and transfer controller 981 receives signals from the header bus 930, the microprocessor access bus 917a, the frame pulse lead 954, an underflow lead 985, and the clock lead CLK26. A cell loss detector

circuit 982 is connected to communicate with the buffer status bus 925 and the read/write pointer access bus 926. A buffer status manager circuit 983 is connected to drive the read/write pointer access bus 926, to communicate with the buffer status bus 925, and to receive signals from DS0/VPTM bus 929 and the local control bus 981c. A buffer read pointer manager circuit 984 is the source of the read addressing information which it asserts on the buffer DS0 read address bus 938 as well as being the source of an underflow interrupt signal on a lead 986. The buffer read pointer manager circuit 984 is connected to drive the underflow lead 985, to communicate via the buffer status bus 925 and to receive signals from DS0/VPTM bus 929 and the local control bus 981c.

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L3: Entry 12 of 28 File: USPT Nov 24, 1998

US-PAT-NO: 5841771
DOCUMENT-IDENTIFIER: US 5841771 A

TITLE: Telecommunications switch apparatus and method for time switching

DATE-ISSUED: November 24, 1998

INVENTOR-INFORMATION:

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Irwin; George Frank	Kanata			CA
Lam; Du-Tuan	San Jose	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
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APPL-NO: 08/ 675179 [PALM]
DATE FILED: July 3, 1996

INT-CL: [06] H04 L 12/52

US-CL-ISSUED: 370/360; 370/375, 370/383
US-CL-CURRENT: 370/360; 370/375, 370/383

FIELD-OF-SEARCH: 370/353, 370/354, 370/360, 370/370, 370/371, 370/372, 370/373, 370/377, 370/386, 370/389, 370/391, 370/395, 370/399, 370/428

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4450556	May 1984	Boleda et al.	370/58
☐	4603416	July 1986	Servel et al.	370/60
☐	4873682	October 1989	Irwin et al.	370/58.1
☐	4893310	January 1990	Robertson et al.	370/110.1
☐	4926416	May 1990	Weik	370/60.1
☐	5119370	June 1992	Terry	370/354
☐	5144619	September 1992	Munter et al.	370/60
☐	5168492	December 1992	Beshai et al.	370/353
☐	5446738	August 1995	Kim et al.	370/395

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0 320 772	June 1989	EP	
0 537 743	April 1993	EP	
94/11975	May 1994	WO	

OTHER PUBLICATIONS

"Prelude: An Asynchronous Time-Division Switched Network", Coudreuse et al., IEEE, 1980, pp. 769-773.
"Asynchronous Time-Division Techniques: An Experimental Packet Newtork Integrating Video-communication", A. Thomas et al., 1984 International Switching Symposium.

ART-UNIT: 272

PRIMARY-EXAMINER: Kizou; Hassan

ASSISTANT-EXAMINER: Bnimoussa; A.

ATTY-AGENT-FIRM: Foley & Lardner

ABSTRACT:

A switch module for time switching telecommunications data includes an input circuit for selecting data samples from a time slot in an input frame of data samples. The selected data samples are arranged into groups of uniform size, each group consisting of at least two data samples. The groups of selected data samples are stored in an orderly manner, in each of as many storage entities as there are data samples in each group. Thereafter in accordance with a predefined sequence peculiar to each of the storage entities, the data samples are simultaneously read out, group by group. An output circuit selects data samples into a selected group of data samples from among each of the readouts of each of the storage entities and transmits each selected group into an output frame of data samples. Hence a sequence of the data samples appears switched in the output frame with respect to the sequence of the data samples as they were stored from the input frame. The switch module as described inherently provides for switching of data samples, the data samples being permitted to occur at a rate faster than a cycle time of switch module operation.

11 Claims, 41 Drawing figures